Solutions and Processes for Removal of Sidewall Residue after Dry Etching

Background of the Invention

Scope

The present invention relates to a novel process for removing sidewall residue after dry etching. The present invention also relates to a novel solution for removing sidewall residue after dry etching.

Current State of the Art

Processes of Integrated Circuit (IC) Manufacturing:

First is deposited a layer of metal, such as Al, on a substrate surface, such as a wafer, then coating a layer of photoresist on it. This is followed by exposure, developing, etching, ion implantation and photoresist removing. Continuous cycles of film deposition, photoresist coating, exposure, developing, etching and removal of photoresist continue until the desired device is achieved.

There are two kinds of photoresist: positive type and negative type. For positive type photoresist, the area of exposure can be dissolved in developer solution. For negative type photoresist, the area of non-exposure can be dissolved in developer solution. The major composition of positive photoresist is resin, such as Novolac resin. The major composition of negative type photoresist is polyisoprene compound. Generally, baking the photoresist layer after exposure is necessary to make sure that cross-linking reaction is done.

After creating basic IC pattern and more sophisticated IC pattern is to be processed on the substrate, the photoresist and sidewall residue must be removed very efficiently and completely. That is by the use of a photoresist stripper, as in US Patent No. 4,917,122 and 4,963,342 described.

In the etching process of VLSI (Very Large Scale Integrated) or ULSI (Ultra Large Scale Integrated) manufacturing, sidewall passivation formed after dry etching can achieve the anisotropic phenomena of etching process, as in J.L. Vossen, et al, J. Vac Sci. Technol. AL. 1453 (1983); J.H. Thomas, et al, Appl. Phys. Lett. 43, 859 (1983), D. Thomson, et al, Appl. Phys. Lett. 146, 1103 (1985), and J.M.E. Harper, et al, J. Electrochem. Soc. 128, 1077 (1981) described. While etching Poly-Si, according to the etching chemistry of Cl_2 or HBr, oxygen is added to enhance anisotropic tendency and selectivity to oxide layer, as in I. Morimoto et al, Digest of papers, Microprocess 202 (1992) described. While etching Poly-Si layer using Cl_2 as etching gas, silicon reacting with chlorine becomes silicon chloride. If oxygen exists, silicon chloride will be oxidized to silicon oxide, as in K.V. Guinn et al, J. Vac. Sci. Technol. B 13, 214 (1995) described. This silicon oxide is the so-called sidewall passivation, which can prevent isotropic etching. The sidewall passivation cannot be removed completely by conventional ozone ashing and hot sulfuric acid process. In the general process, wafers after treatment of ozone ashing and hot sulfuric acid still need to be immersed in diluted HF solution. The time of immersion cannot last too long to avoid attacking bottom oxide layer. Although the residue can be removed by special stripper, it is not convenient enough. Therefore the process of removing sidewall residue after dry etching should be improved.

Summary of the Invention

The present invention relates to a novel solution in which a certain amount of fluorine-containing compound, preferably hydrogen fluoride and ammonium fluoride, is added into sulfuric acid. This solution can completely remove sidewall residue which is formed after dry etching.

The invention also relates to a novel process by which sidewall residue after dry etching can be completely removed by the above mentioned novel solution.

Brief Description of the Drawings

Fig.. 1 shows the flow chart of the conventional and the novel process used in IC manufacturing process. Fig. 2 shows the magnified picture of a wafer treated with the conventional process and the magnification is 13,100 times.

Fig. 3 shows the magnified picture of a wafer treated with the novel process and the magnification is 11,000 times.

Detailed Description of the Invention

The processes of IC manufacturing can be described as follows. First of all, cleaning wafer surface, then depositing SiO_2 and Poly-Si films on it. After that, photoresist coating, exposure, developing, etching and photoresist stripping processes are done. Fig. 1 shows the flow chart of the process.

Conventionally photoresist and sidewall residue are removed by ozone ashing and hot sulfuric acid, but they cannot be removed completely (Fig. 2). Following immersion into diluted HF solution or special strippers is required.

The present invention is a process on which by addition of fluorine-containing compound into sulfuric acid, controlling the ratio of sulfuric acid to fluorine-containing compound, complete removal of sidewall residue without the need for diluted HF and special strippers can be achieved (Fig. 3). The process is simpler and can reduce process steps to only one. Fig. 1 shows the flow chart of the process.

The invention uses a novel solution to remove sidewall residue formed after dry etching, which comprises sulfuric acid and a fluorine-containing compound, in the range of from 10:1 to 1000:1 by weight, preferably in the range of from 100:1 to 700:1, most preferred in the range of from 300:1 to

500:1. The fluorine-containing compound is composed of fluorine ion and mono-charge cation, such as alkaline metal cation, ammonium cation and hydrogen ion, preferably hydrogen fluoride and ammonium fluoride. The novel solution is prepared by adding hydrofluoric acid or ammonium fluoride into sulfuric acid, and then mixing it with hydrogen peroxide at temperature 100-140 °C, preferably 120 °C. The above mentioned chemicals can be commercially available ones like H_2SO_4 96 %, H_2O_2 31 %, HF 49 %, NH_4F 40 %.

While using the new process to remove sidewall residue after dry etching, both organic and inorganic, such as SiO_2, compounds can be removed. It can be implemented without increasing difficulty of the process. Just after dry etching and ozone ashing, put wafer into the pre-mixed solution of sulfuric acid and fluorine-containing compound, and maintaining operation pressure at 1 atm, temperature at 00-140 °C (preferably 120 °C) for 10 min. The photoresist and sidewall passivation formed after dry etching can be removed completely and the novel solution does not affect the film of poly-Si, and only slightly etching the bottom oxide layer (less than 1 Å/min). After dry-etching process, the wafer is put into the reaction chamber in which the ozone ashing process is done. During this process, ozone decomposes into oxygen and oxygen atoms which react with large amounts of carbon atoms in the photoresist under high temperature condition and then form CO_2. By detecting the amount of CO_2 one can know whether ozone ashing reaction completes or not.

The new process is simple, speedy, and does not need to use strippers or other solutions any more. Manufacturing cost for IC devices can be reduced significantly. Both feasibility and practicability of this new process are high. The process is suitable for several kinds of photoresists including g-line, i-line, Deep UV, E-beam and X-ray resists.

The following examples are further explanations of the invention. However, the scope of this invention is not limited to these examples. All possible substitutes and adjustments done by people who are familiar with this technique are belonging to the application and range of this invention.

Example 1

The photoresist used in the process is FH-6400L g-line photoresist (Fuji-Hunt). Exposure is done by PAS 2500/10 g-line stepper (ASM). Developer used in the process is FHD-5 developer containing TMAH 2.38 % (Fuji-Hunt). Developing time is 60 sec. The ECR (Electron Cyclotron Resonance) etching machine is used for etching 3000A of Poly-Si. The plasma is produced by using Cl_2 (95 sccm), O_2 (5 sccm) and 250 W microwave. DC Bias is provided by 35 W of RF. Pressure in the chamber is 3 mTorr while temperature is -20 °C. Etching time is 70 sec. The etching rate for Poly-Si is 2612 Å/min for Poly-Si, 26 Å/min for SiO2, 766 Å/min for photoresist. As for selectivity, the ratio of Poly-Si to SiO2 (2612/26) is 100 while Poly-Si to photoresist (2612/766) is 3.4.
(sccm - standard cubic centimeter per minute)

Comparative Example

After dry etching, conventional process is used to remove photoresist. At first, the photoresist is removed by ozone ashing which is done inside the chamber, one wafer per time at temperature of 200-300 °C. At this temperature, decomposed oxygen from ozone reacts with the carbon of photoresist and forms CO_2. Then the wafer is immersed into mixed solution of sulfuric acid and hydrogen peroxide at 120 °C for 10 min. After this treatment, the wafer is inspected by SEM (Fig. 2). At this stage, only photoresist can be removed while sidewall passivation after dry etching cannot be removed completely. Diluted HF or special stripper is needed for further treatment.

Example 2

After dry etching, present novel process is used to remove photoresist. At first, photoresist is removed by ozone ashing which is done in the same way as the comparative example. Then the wafer is immersed into mixed solution of sulfuric acid, hydrofluoric acid and hydrogen peroxide at 120 °C

for 10 min. The ratio of sulfuric acid + hydrofluoric acid to hydrogen peroxide is 3:1 by volume. After this treatment, the wafer is inspected by SEM (Fig. 3). It is obvious that photoresist and sidewall passivation after dry etching are removed completely by this single step without affecting Poly-Si and bottom SiO_2 layer.

Example 3

After dry etching, present novel process is used to remove photoresist. At first, photoresist is removed by ozone ashing which is done in the same way as the comparative example. Then the wafer is immersed into mixed solution of sulfuric acid, ammonium fluoride and hydrogen peroxide at 120 °C for 10 min. The ratio of sulfuric acid + ammonium fluoride to hydrogen peroxide is 3:1 by volume. After this treatment, the wafer is inspected by SEM. It is obvious that photoresist and sidewall passivation after dry etching are removed completely by this single step without affecting Poly-Si and the bottom SiO_2 layer.